ASMEX.448A PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number: 10/800,390 Confirmation Number: 7151

Applicant: Brabant et al.

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Commissioner for Patents
Post Office Box 1450
Alexandria, Virginia 22313-1450

DECLARATION OF DR. MATTHIAS BAUER UNDER 37 C.F.R. § 1.132

Sir:

I, Dr. Matthias Bauer, declare as follows:

1. I have received a Diploma in Physics from Eberhard-Karls-University, Tuebingen (Germany) and a Ph.D. in Electrical Engineering from University of Stuttgart (Germany). Since 1996, I have performed a substantial amount of research in the following fields: homo- and hetero-epitaxy of group IV materials (Si, SiGe, Ge, SiGe:C, Si:C); growth of ultra-thin, highly relaxed SiGe buffer layers on Si as

virtual substrates for tensile strained Si channels of NMOS devices; amorphous to epitaxial phase transition at very low growth temperatures; formation of epitaxial films by solid phase epitaxy and recrystallization of amorphous films; and epitaxial growth for electrical device fabrication. Based on this and other experience, I consider myself skilled in the art of fabricating semiconductor devices, and more specifically, in the art of depositing epitaxial films such as epitaxial germanium and silicon germanium films.

2. I am a co-Inventor of the invention claimed in U.S. Patent Application 10/800,390, which was filed on 12 March 2004, and which is referred to herein as "the '390 Application".

3. The '390 Application discloses, among other things, methods for depositing an epitaxial germanium-containing layer. In one embodiment, an epitaxial germanium-containing layer is deposited by initially heating a single crystal silicon structure to a first temperature. The single crystal silicon structure is then cooled to a second temperature during a cooling period. A surface active compound is contacted with the single crystal silicon structure during at least a portion of the cooling period. An epitaxial germanium-containing layer is deposited over the single crystal silicon structure at the second temperature.

4. I am familiar with the course of prosecution of the '390 Application, including the Office Action mailed on 24 January 2006, in which European Patent Application Publication EP 0 858 101 A2 ("Aoyama") and U.S. Patent 6,875,279 ("Chu") were relied upon.

5. I have carefully studied Aoyama. Aoyama discloses methods for manufacturing a Si/SiGe super lattice structure using epitaxial growth techniques. In what Aoyama characterizes as the "Second Embodiment", a method is disclosed wherein a substrate is first heated to a temperature of 600°C or more, at which point a silicon epitaxial layer is deposited. The substrate is then cooled to 600°C or less, at which point a silicon epitaxial layer that contains germanium is deposited. See Aoyama at column 7, lines 17–33.

6. As far as I can discern, Aoyama contains no teaching or suggestion that any deposition or provision of a surface active compound occurs during the period of time when the substrate is cooled.

7. I have carefully studied Chu. Chu discloses methods for manufacturing silicon and/or silicon germanium semiconductor structures. In what Chu characterizes as "Example 1", a method is disclosed wherein a silicon epitaxial layer is grown at a temperature between 700°C and 950°C in a reaction chamber. This layer is then rapidly cooled to a reduced epitaxial growth temperature by using a cryogenic pump to reduce the pressure in the reaction chamber to 10^{-8} mtorr or less. The cryogenic pump is deactivated, and silane flow is initiated to grow a low temperature epitaxial film comprising silicon, germanium, and/or silicon germanium. See Chu at column 7, line 55 through column 8, line 5.

8. As far as I can discern, Chu contains no teaching or suggestion that any deposition or provision of a surface active compound occurs during the cooling period.

9. At the time the invention claimed in the '390 Application was made, an ordinarily-skilled artisan would not have expected that modifying either Aoyama or Chu to continue the growth step during cooling would yield successful results because dynamic temperature fluctuations during cooling would have been expected to detrimentally affect the uniformity and thickness of the deposited film.

10. Before the invention claimed in the '390 Application was made, an ordinarily-skilled artisan would understand that active compound flows would be paused during the temperature ramp in the context of a dual-temperature deposition sequence. This is because in semiconductor processing generally, and in chemical vapor deposition specifically, it is important to precisely control processing parameters. For example, it is important to precisely control the duration and the temperature that reactants are exposed to a surface in order to precisely predict deposited film properties. Therefore, at the time the invention claimed in the '390 Application was made, it was generally understood that deposition processes should be conducted at stable temperatures so as to provide precise control over the processing parameters.

11. Both Aoyama and Chu teach methods wherein cooling occurs between a high temperature deposition step and a low temperature deposition step. Based on the ordinarily-skilled artisan's preference for deposition at stable temperatures,

as set forth in Paragraph 10 of this Declaration, an ordinarily-skilled artisan would read the disclosures of Aoyama and Chu with the assumption that no surface active compound should be provided during cooling without some specific teaching to flow reactants during cooling. Neither Aoyama nor Chu appears to contain such a specific teaching.

12. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued therefrom.

Dated: 3/24/06 By: _____
Dr. Matthias Bauer

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